In the Claims:

Claims 1 – 16 (canceled)

17. (currently amended) A trench structure formed in a semiconductor substrate comprising:
an upper portion of said trench having an upper polygonal cross section;
a lower portion of said trench having a lower polygonal cross section comprising four straight main sides oriented with an angular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; ~~and~~ connecting lines connecting said inner corners with said main sides; and said lower polygonal cross section having a greater number of sides than said upper polygonal cross section.

18. (currently amended) A capacitor formed in a trench in a semiconductor substrate comprising:
an upper portion of said trench having an upper polygonal cross section;
a lower portion of said trench having a lower polygonal cross section comprising four straight main sides oriented with an angular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; ~~and~~ connecting lines connecting said inner corners with said main sides; said lower polygonal cross section having a greater number of sides than said upper polygonal cross section; a node dielectric disposed on interior surfaces of said lower portion of said trench; and a conductive center electrode disposed within said trench and abutting said node dielectric.

19. (canceled)

20. (original) A capacitor according to claim 18, further comprising a transistor formed within said upper portion of said trench connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, said capacitor and said transistor together thereby forming a DRAM cell.

21. (new) A trench structure formed in a semiconductor substrate comprising a trench having a polygonal cross section comprising four straight main sides oriented with an angular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; connecting lines connecting said inner corners with said main sides; and said polygonal cross section having a number of sides greater than four.

22. (new) A capacitor formed in a trench in a semiconductor substrate comprising
a trench having a polygonal cross section comprising four straight main sides oriented with an angular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; connecting lines connecting said inner corners with said main sides; a node dielectric disposed on interior surfaces of a lower portion of said trench; and a conductive center electrode disposed within said trench and abutting said node dielectric; and said polygonal cross section having a number of sides greater than four.